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DSTO

A Microprocessor-Based Gradient Analyser for F/A-18 Bulkhead Spectrum Loading

Leopold Sponder

DSTO-TR-0546

DEPARTMENT OF DEFENCE

DEFENCE SCIENCE AND TECHNOLOGY ORGANISATION

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Maritime Platforms Division
Aeronautical and Maritime Research Laboratory

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ABSTRACT

This report describes a specially designed instrument that was used during a full scale fatigue test of an F/A-18 bulkhead to support the acquisition and analysis of acoustic emission (AE) data for the investigation of crack initiation and growth. This device, developed by the author, comprises both hardware and software and generates binary data in real time that indicates the sign of the gradient of an applied spectrum load signal. This design overcomes the inherent limitations of conventional analog slope detection methods applied to slowly varying aperiodic waveforms.

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Executive Summary

As part of the total commitment to the maintenance and airworthiness assurance of the F/A-18 fleet, Australia and Canada have undertaken a collaborative program (IFOSTP, International Follow on Structural Fatigue Test Program) to analyse the structural integrity of the F/A-18 by loading the structure in ways that simulate flying conditions.

Cracks in the airframe generate high frequency sound waves (acoustic emission) when loads are applied and these signals can be collected and analysed to identify when and where cracks have formed and also the rate at which they are propagating. The detection and sizing of these cracks and other damage that result from the repeated loading of the airframe are critical to the assessment of structural integrity.

This report describes a specially designed instrument that analyses the slope of the load signal during fatigue loading which is used with other data to help discriminate against sounds that may emanate from the structure or loading system but which are not themselves caused by cracks. This in turn improves the reliability of the acoustic emission method for the assessment of cracks in the airframe.

Authors

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Mr. Leopold Sponder has a BSc.(Hons) degree in Physics and also a Master of Science degree, specialising in X-ray diffraction, from the University of Melbourne.
He joined DSTO at the Aeronautical and Maritime Research Laboratory in 1987 as an Experimental Officer Class 1 and has since worked in the fields of non-destructive inspection research including ultrasonics, laser ultrasonics, acoustic emission, magnetic methods and X-ray backscattering. He has also worked in the area of structural reinforcement. His principal skills include x-ray diffraction/crystallography, professional photography, public speaking, electronics and instrumentation, data acquisition methods, computer modelling, computer programming in several languages, mechanical testing and specialised metallurgical applications.
He is currently studying for his second Master of Science degree in the Communication and Electronic Engineering Department at the RMIT University

Contents

1. Introduction

Information extracted from acoustic emission signals during fatigue testing can yield important information about crack initiation, location, and subsequent growth rates. In addition to crack related acoustic emission, however, other acoustic sources such as the rubbing of bolts and fixtures, fretting etc., will contribute as background noise. Fortunately AE events which occur exclusively on load maxima in a positive load cycle are consistent with the known characteristics of crack related sources [4] so that the combined load and load gradient information *in situ* is useful for isolating these specific acoustic events.

A large amount of acoustic emission data can be generated during fatigue testing especially when, as is often the case, testing occurs over periods of weeks or months. This places considerable system demands on data storage, speed of acquisition, cost and reliability. Furthermore, the more data collected the greater the time required for post-processing which may lead to problems if results are required in real (or near real) time. By using the load gradient for gating out extraneous acoustic emission events it may also be possible to avoid acquiring AE data from extraneous noise sources which do not result directly from crack propagation.

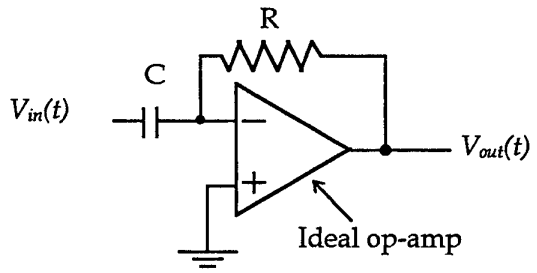
This instrument was designed by the author for the F/A-18 bulkhead fatigue testing program at AMRL which began in late 1988. Acoustic emission data from a critical region of the bulkhead was post-processed to investigate crack initiation and crack growth rates. The signal provided by this instrument was acquired as one channel in a multi-channel data acquisition system[1] to enhance and simplify the post-processing of the data.

This device outputs a digital logic level (TTL), ie. logic high or logic low, to indicate the state of the gradient of a signal in real time. A positive or zero gradient is represented by logic high and a negative gradient by logic low. This device is not limited to analysing load spectra but can, at least in principle, be used to monitor any arbitrary analog signal in real time where only the sense (+ or -) of the gradient is required.

2. Problems for Conventional Designs

The usual method for obtaining the gradient of an analog waveform uses a differentiator circuit of the general type shown below.

[1] Dunegan DART Acoustic Emission system



With this type of circuit the output voltage is given by:

$$V_{out} = -RC \frac{dV_{in}}{dt}$$

In the case of an aircraft flight spectrum both the amplitude of the signal peaks and the gradient of the load waveform vary with time. Consequently V_{out} undergoes large amplitude changes and this places very high demands on the dynamic range capability of the analog circuitry. Furthermore, at very low frequencies (i.e. <1 Hz), within the normal envelope of the flight spectrum, dV_{in}/dt can be very small so that to accommodate this end of the spectrum with an acceptable signal-to-noise (S/N) ratio for V_{out} the multiplier, RC, must be made large. This, however, also tends to exacerbate the already high noise sensitivity inherent in this type of circuit and taken together these problems generally make this design approach impractical for this type of signal.

Nonetheless, because of its simplicity a circuit of the conventional type described above was constructed but as anticipated all attempts at tailoring the circuit to meet our requirements failed. It was, therefore, ultimately abandoned for the necessarily more complex but more suitable system which is described below.

3. The Author's Design

This design combines an inexpensive microprocessor with some supporting hardware and software to create a simple to operate stand-alone system. Basically, the device takes the load signal on its input, converts it into digital form, calculates the sense of the gradient in real time, and outputs the result in a digital HIGH/LOW form for recording or further processing.

A functional schematic is shown in Figure A1. There are three main sections consisting of:

- Analog circuitry, comprising a linear op-amp with adjustable gain (input impedance ~ 100 kohms) and an active second order (-40 dB/decade) Sallen and Key low pass (f_c ~ 30 Hz) filter.

- Digital circuitry, consisting of an analog-to-digital converter (ADC), 6522 8 bit I/O interface port, and a SYM-1[2], 6502-based microprocessor card operating at a clock frequency of 1 MHz.
- The software, written in machine language, to control in real time the overall process of acquiring and digitising the load waveform, analysing the gradient, and generating the result.

3.1 Circuit Description

With the exception of the microprocessor CPU (central processing unit) and its commercially designed subsystem (see ref [2]) all other supporting circuitry was developed at AMRL. It consists of three main stages; a buffer/amplifier, signal conditioner and 8 bit analog-to-digital converter. The circuit schematics are given in Figures A2 and A3.

3.1.1 Stage 1: Buffer/Amplifier

Stage 1 uses a linear op-amp to buffer and amplify the analog signal. To accommodate a range of signal amplitudes gain adjustment is provided via a 250 kohm trimpot (VR1). The gain, while not actually critical, should be set high enough to take advantage of the full precision of the ADC without over-ranging the ADC or causing the signal to clip. The optimal gain occurs when the full span of the load signal produces an output swing at the SIG. OUT connector which lies just within +/- 5V peak-to-peak (p-p). The gain is variable between 0 and about 2.5 with the listed components.

3.1.2 Stage 2: Signal Conditioner

This stage consists of a low pass second order Sallen and Key filter to band limit the analog signal prior to it being presented to the ADC. The cutoff frequency ($f_c \sim 30$ Hz) was chosen by trial and error to provide effective noise immunity while also ensuring negligible phase shift (i.e. time delay) at the highest frequency likely to be important (~ 1 Hz).

3.1.3 Stage 3: Analog-to-Digital Converter

In this stage a monolithic analog-to-digital converter (ADC0801) converts the filtered waveform into an 8 bit data word. In this design the ADC is used in its free running mode at a frequency of about 500 khz and presents the digital data to a 6522 I/O port

[2] SYM-1 is a Trademark of Synertek Systems Corporation

on the microprocessor card. Data appearing on the inputs to the 6522 are stored in a hardware register which is then read under the control of the acquisition software (program GRAD).

3.2 Operation

The signal being monitored is input at the connector labelled SIG IN and a TTL signal representing the sense of the gradient is presented at the connector labelled SLOPE. An LED (light emitting diode) is provided beside this connector to give a visual indication of the state of the output i.e. HIGH (LED on) or LOW(LED off). Another connector, labelled AMP OUT, gives the signal at the output of the first analog stage and is used as the test point for setting the gain of the first stage, described above.

To get the system running after applying power requires just two steps:

- Starting the ADC and
- Running the GRAD program

To start the ADC apply power and then press the front panel button labelled ADC. The GRAD software is then started by pressing the button labelled PROGRAM. From then on the unit will operate continuously until the mains power is interrupted or the program is deliberately halted by the user.

3.3 The Control Software

The software, known as GRAD, controls the operation of the ADC, acquires its 8 bit data through a 6522 I/O port, carries out the necessary data processing to calculate the sense of the gradient and sends the result to a second I/O port as a TTL logic level HIGH/LOW. The output from this I/O port can then be accessed via a connector on the instrument front panel. The software is written in 6502 machine language to enhance the execution speed and has been recorded permanently on a 2732D EPROM (Erasable Programmable Read Only Memory) for ease of use and to make the instrument completely self contained. When started the program loops continuously analysing the input signal and updating its output until interrupted by the user. The flow diagram for the code appears in Figure A4 and the detailed code listing is given in Appendix B.

The GRAD program periodically instructs the 6502 microprocessor to read the 6522 I/O port (Port A) to acquire the most up to date signal voltage data. This data is then added to the data acquired from prior samples and stored in RAM (Random Access Memory). This data sum is stored as two successive bytes to give a range of 16 bits (0 to 65535) and these are referred to, collectively, as bin 2. After summing a fixed number of samples a second set is initiated as bin 1 and when an identical number of samples have been read the two bins are compared. The result is then presented as a

logic level on one I/O line of the second I/O port (Port B). If the result is positive or zero the output is given as a logic LOW and vice versa. Since this logic level is inverse to the conventional mathematical sense it then passes through an inverter which also acts an electrical buffer. This inverted signal is then passed to the connector labelled SLOPE on the unit's front panel so that logic HIGH represents a +ve or zero gradient and LOW represents a -ve gradient.

Parameters which may be varied through the GRAD software include the time interval between successive samples and the number of samples needed to fill each bin. The latter is equivalent to introducing an analog low pass filter and may be useful for reducing the effects of random electrical noise. In general the greater the number of samples the greater the accuracy and consistency of the gradient assessment but with the drawback that the more samples required the greater the time delays involved. Long intervals will produce a noticeable phase lag on the output of this device when compared with the true instantaneous gradient.

Errors can also occur due to finite numerical precision. For example, when analysing slowly changing signals over a relatively short time interval the accumulated data in each of the two bins will be numerically close. Where the difference is only of the order of the digital precision, the process by which the gradient is calculated becomes much more sensitive to the effects of noise and the gradient can easily be assessed as having the wrong sign. In extreme cases, where the gradient is very close to zero, the output of this device may become erratic, appearing to oscillate between HIGH and LOW.

Under these conditions simply increasing the time interval between successive samples can improve the performance of this type of device because the signal then has more time to change appreciably. This approach is especially effective where the signal/noise ratio is poor but it must be noted that this method cannot be extended indefinitely because it can lead to unacceptable time lag in a real time system such as this.

3.4 Performance Analysis

The analog part of this system is fixed except for the gain which can be optimised by ensuring that the dynamic range of the load signal just lies within the range of both the amplifiers and ADC converter.

Optimising the performance of the digital part of this system is a matter of understanding the limitations imposed by the method of sampling. In particular both the sampling rate and the number of samples per bin should neither be too high nor too low (for the type of waveform being monitored) and with this design there are just two software parameters that need to be adjusted to achieve optimal performance.

In the following analysis it is assumed that the accumulated time delays in the signal path between the signal being measured and the output of this device are negligible. This includes phase delays in the analog electronics and gate propagation delays in the digital elements.

We also assume that the microprocessor never samples the same data twice. One way to achieve this is to ensure that the ADC converter is converting samples faster than the rate at which the microprocessor reads the I/O port. Alternatively, as in this system, data is only read from the port when the ADC signals that a conversion is complete and because the conversion rate is around 500,000 samples per second (i.e. about once every two CPU clock cycles) in practice here the CPU never has to wait for new data.

As a starting point for calculation and as a worst case analysis we assume that the signal waveform is sinusoidal and of constant frequency so that it may be represented as:

$$S(t) = A\sin(2\pi ft) \qquad 1.$$

where S(t) represents the magnitude of the waveform at time t, A is the amplitude, and f is the frequency. Where the waveform is not sinusoidal, equation 1, above, would still be used with S(t) chosen to represent the lowest Fourier component of the waveform being used.

The instantaneous gradient is then:

$$S' = \frac{dS}{dt} = 2\pi fA\cos(2\pi ft), \qquad f = \frac{1}{T} \qquad 2.$$

so that the incremental change in the signal over a time interval given by *dt is*:

$$dS = S'\,dt = 2\pi fA\cos(2\pi ft).dt \qquad 3.$$

Condition 1: The time required to determine the gradient must be within an acceptable limit

Since it takes a finite time to determine the gradient by multiple point sampling there needs to be set a maximum time for the delay. A reasonable value is that the total time taken should not exceed around 10 % of the period of the waveform as this is comparable to the confidence limits for AE data as a whole. This condition, expressed mathematically, becomes:

$$\frac{T_c}{T} \leq 0.10 \qquad 4.$$

where T is the period of the waveform assumed to be cyclic and T_c is the period between successive output states and is the sum of three components:

$$T_C = T_B + T_S + T_O \qquad 5.$$

T_B is the time to accumulate a full set of samples into a bin. T_S is the software overhead incurred, (i.e. time delay) after the last sample has been accumulated in bin 2, to

compare data bins (1 and 2) and send the result to Port B. T_O is a further software overhead that occurs between when the gradient result is output to Port B and before data can again begin to be sampled. All times are in seconds.
By analysing the GRAD code and taking into account the number of clock cycles per instruction we find that T_B is given by:

$$T_B = \left(LIMIT \times \left(51 \times DVAL + 77\right)\right) \times \frac{1}{f_{CPU}} \quad LIMIT \geq 1,\ DVAL \geq 1 \qquad 6.$$

DVAL is a software parameter in GRAD which controls the duration of a timing loop that sets the interval between the successive samples in a given bin. LIMIT is a parameter which sets the number of samples required for a full bin and both are measured in numbers of CPU clock cycles. f_{CPU} is the CPU clock frequency in Hertz.

From the GRAD code we also get a range for the time (T_S + T_O) since the actual number of CPU cycles involved depends on the exact nature of the calculations which are performed.

$$\frac{47}{f_{CPU}} \leq \left(T_S + T_O\right) \leq \frac{60}{f_{CPU}} \qquad 7.$$

Condition 2: Signal changes must be greater than the digital resolution

The smallest meaningful signal changes that can be can be measured are around 1% of the amplitude for signal levels that have been optimised to fit just within the range of the ADC. Under these circumstances a 1% confidence level corresponds to a precision equivalent to about twice the least significant bit (8 bit resolution). The condition is:

$$|dS| \geq 0.01A \qquad 8.$$

Result for Condition 1

Combining equations 4, 5, 6, and 7 we get:

$$LIMIT \times \left(51 \times DVAL + 77\right) + 60 \leq 0.1T \times f_{CPU} \qquad 9.$$

where in this instance to be conservative the maximum value $(T_S + T_O) = \frac{60}{f_{CPU}}$ has been used.

Result for Condition 2

Combining equations 3, 5, 6, 7, 8 and recognising that $dt = T_C$ we get:

$$dS = 2\pi f\left(LIMIT \times (51 \times DVAL + 77) + 47\right)\left|\cos(2\pi ft)\right| \times \frac{1}{f_{CPU}} \geq 0.01 \qquad 10.$$

where we have used the conservative case that $(T_S + T_O) = \frac{47}{f_{CPU}}$.

On rearranging we get:

$$\left(LIMIT \times (51 \times DVAL + 77) + 47\right) \geq \frac{0.01 \times f_{CPU}}{2\pi f\left|\cos(2\pi ft)\right|} \qquad 11.$$

Combining the results for eqs. 9 and 11 we get finally:

$$D_{\min} \leq LIMIT \times (51 \times DVAL + 77) + 47 \leq D_{\max} \qquad 12.$$

$$D_{\min} = \frac{0.01 \times f_{CPU}}{2\pi f\left|\cos 2\pi ft\right|}, \qquad D_{\max} = 0.1T \times f_{CPU}$$

D_{min} expresses the condition that there is a minimum sampling period below which changes in the signal voltage are less than the digital resolution and that the lower the frequency the greater the time required. In a system with greater than 8 bit resolution this time will be correspondingly less.

D_{max} represents the maximum acceptable time interval between bins at a given signal frequency and CPU clock frequency.

For the situation where the waveform is not sinusoidal as in the case of the F/A-18 load spectrum we may substitute for the signal frequency, f, the equivalent Fourier components ranging in this case from about 0.1 Hz to about 1 Hz.

To maximise the performance of this device we must consider the range of frequencies in the signal being measured and then select parameters which give the best overall balance between response time and accuracy. Consequently for an arbitrary waveform with frequency components ranging from about 0.1 Hz to 1Hz for D_{min} the worst case occurs when $\cos(2\pi ft) = 1$ and $f = 0.1$ Hz whereas for D_{max} we require the maximum frequency which is f = 1 Hz (i.e. $T = 1.0$ second). In the case of the microprocessor system we are using the system clock frequency is fixed at $f_{CPU} = 10^6$ Hz so that the approximate limits are:

$$397 \leq \left(LIMIT \times (51 \times DVAL + 77) + 54\right) \leq 1 \times 10^5 \qquad 13.$$

This simple result means that the software parameters LIMIT and DVAL can be set independently to give the best subjective performance provided that the term in parentheses, above, remains approximately within the range specified above.

The analysis presented above is, of course, only intended as a guide and does not take account of external factors in the performance of the device such as electrical noise etc.

3.5 Program Variables

Most of the user configurable parameters that GRAD uses are stored at RAM addresses in the range hex 0000 to hex 0006 (refer to GRAD listing, Appendix B). When GRAD is started it copies default parameters stored in EPROM into these RAM locations and thereafter it uses these parameters during execution. It is possible to alter any of the parameters after execution has begun by interrupting the program, modifying the parameter(s), as described below, and then continuing execution from the last completed instruction. The procedure is given below:

- Apply power to the unit.
- Start the ADC by pressing and releasing the ADC button on the front panel.
- Start program GRAD by pressing the PROGRAM button on the front panel.
- Lift the top panel from the unit to gain access to the microprocessor board inside. On the board is a membrane type keyboard which controls most of the functions of the microprocessor itself, including the operating system software. Press the key labelled ON which is directly above the word DEBUG. This halts execution of program GRAD and places the microprocessor in DEBUG mode which allows access to RAM and certain system functions. An LED to the left of the keypad will light to indicate that the microprocessor has correctly entered DEBUG mode.
- Press the MEM key followed by the four hexadecimal digits which represent the memory address where the required parameter is stored. Finally, press the key labelled CR (carriage return) after which the display above the keypad will show the address and data as follows. The system is now ready to accept new data at the address shown.

Address (4 digits)				Data (2 digits)	
MSD*			LSD*	MSD*	LSD*

* MSD - most significant digit. LSD - least significant digit

- Press two digits (MSD followed by LSD) to enter the new data value. The address will increment by one.

- Repeat the process until all changes have been made.
- Press CR again to complete the data entry.
- When all the required changes have been made press the key labelled OFF below the word DEBUG. The DEBUG indicator LED will extinguish.
- Finally, press the keypad labelled GO followed by CR to continue execution of program GRAD from the last completed instruction with the new parameters.

3.5.1 Optimising Program Parameters

This system was optimised for the bulkhead trials which were completed at AMRL in April 1990. In future work, if required, the system parameters, LIMIT and DVAL, can be altered by trial and error to meet the requirements of the particular test program. The recommended approach is to start with LIMIT = 1 and DVAL about 5 and observe the effect on the steeper gradients as LIMIT is increased. The gradient monitor's output should become more faithful as LIMIT is increased and the range of gradients for which the output is correct should also increase. Stop increasing LIMIT when a reasonable subjective result is obtained. From the value obtained for LIMIT calculate the approximate maximum value for DVAL given by eq. 12.

The parameter, DVAL, has it's greatest effect on the parts of the signal with a lower gradient. Increase DVAL for best effect on the lower gradients within the limits imposed by eq. 12.

Repeat the process with different starting values as necessary to get the best overall result under the conditions being used.

4. Results

Appendix A6 (A, B) contains photographs taken from a storage oscilloscope showing intervals from representative load sequences as actually applied to an F/A-18 bulkhead. The upper trace on each photograph shows the applied load and the lower trace is the signal output from the gradient analyser. The time interval represented by these frames is about 20 seconds and the results show quite clearly that the gradient analyser gives a faithful assessment of the gradient and with acceptable phase error. These photographs were taken using the parameters in GRAD listed below and these were the ones finally selected for the actual AE test program.

LIMIT: hex 60 (decimal value 96) DVAL: hex 15 (decimal value 21)

$$LIMIT \times (51 \times DVAL + 77) + 47 \cong 110{,}000$$

5. Conclusion

Microprocessor based digital sampling and processing of an analog waveform for gradient sense monitoring has proved effective for analysing the spectrum load signal used in a full scale fatigue program of an F/A-18 bulkhead. This technique is especially useful for relatively low frequency pseudo-random waveforms since it overcomes the major limitations of conventional analog designs.

The device presented here contributed significantly to the AE program at AMRL and has proved itself to be effective and reliable in the fatigue testing work. The potential exists for further enhancing the performance of this stand-alone system through the use of a faster microprocessor and a higher resolution A/D converter.

Acknowledgments

I wish to acknowledge the excellent technical support and general advice given by Mr. J. McCardle.

I also wish to thank Ms. S. Bowles for her encouragement, participation and general support in this task.

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3. Assembly Language Programming. Lance A. Leventhal. Osborne / McGraw Hill. © 1979. ISBN 0-931988-27-6.

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Appendix A

Diagrams and Photographs

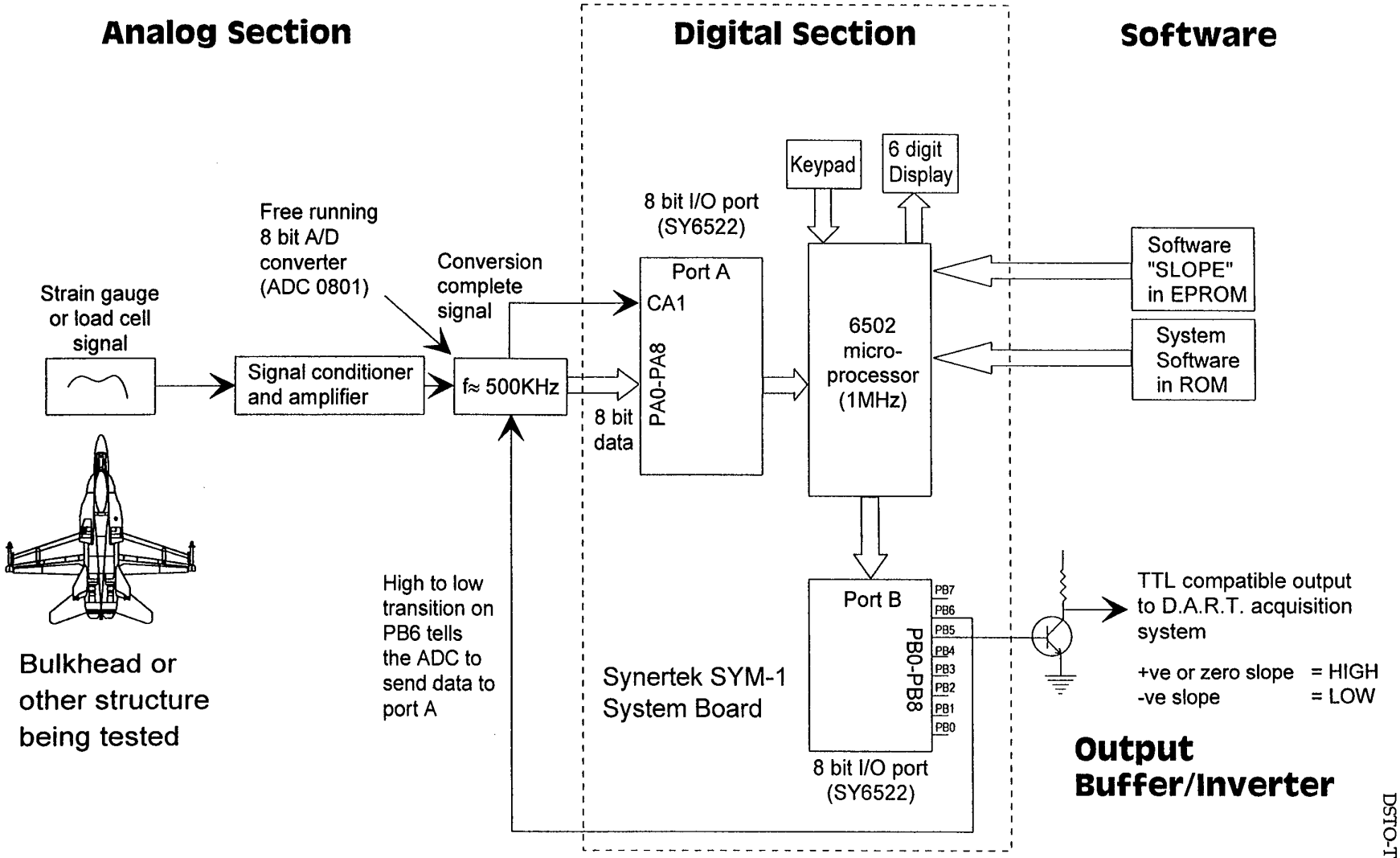


Figure A1. Functional block diagram of the gradient monitor

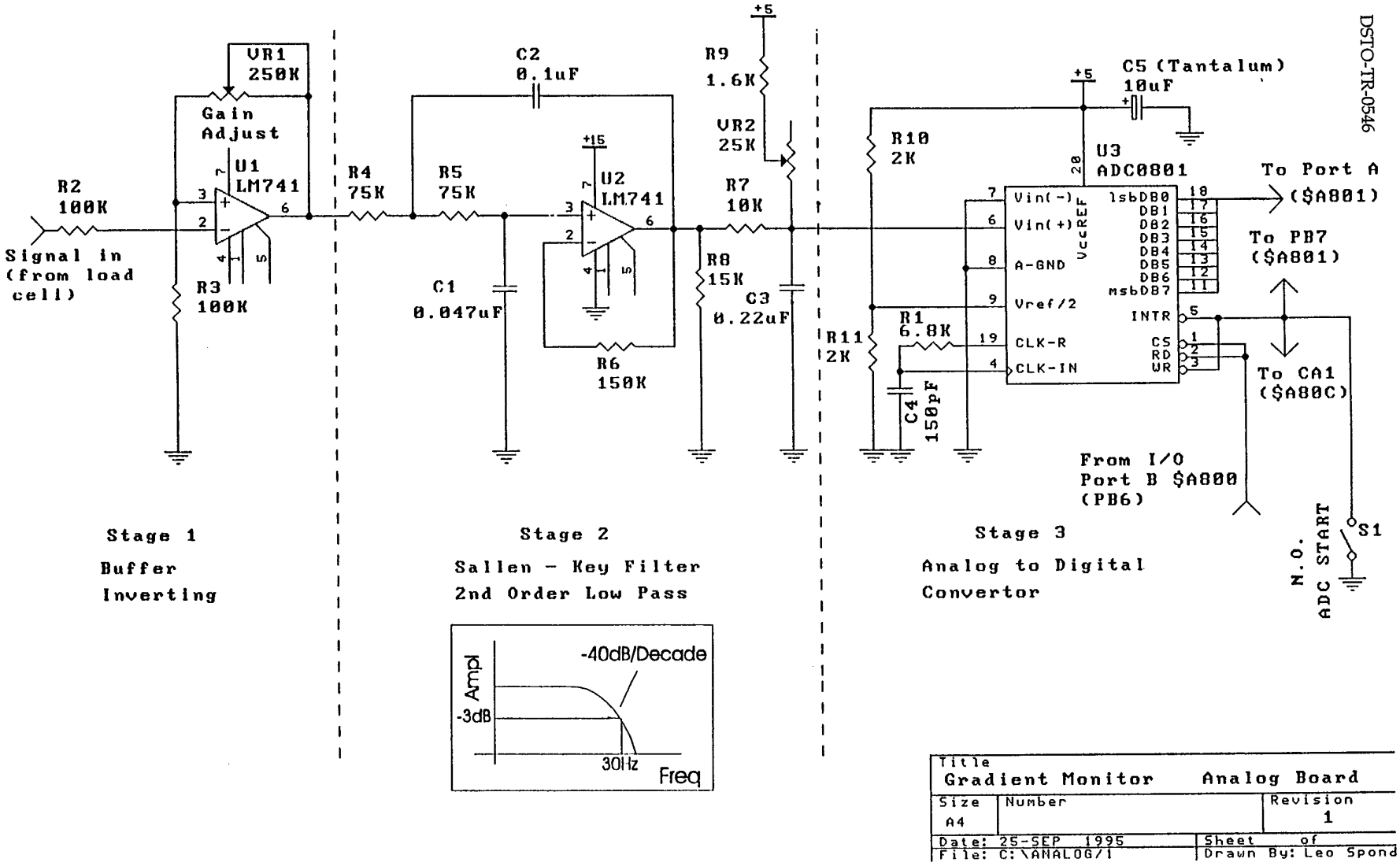


Figure A2. Signal conditioner and A/D converter circuits.

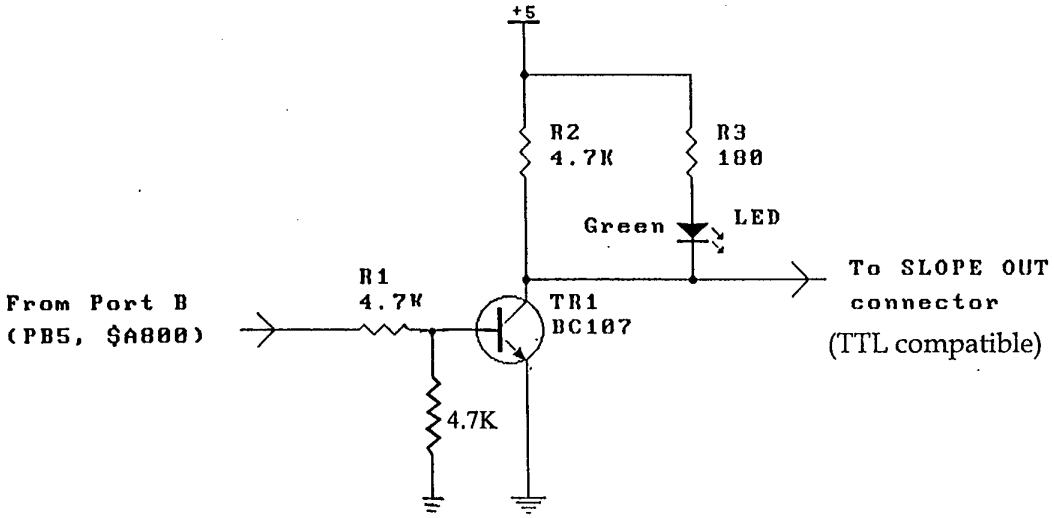


Figure A3. Inverter/buffer circuit from Port B, bit 7 (PB7) to SLOPE output.

Title		
Gradient Monitor		Output Stage
Size: A4	Number	Revision: 1
Date: 25-SEP 1995		Sheet of
File: OUTPUT/1		Drawn By: L. Sponder

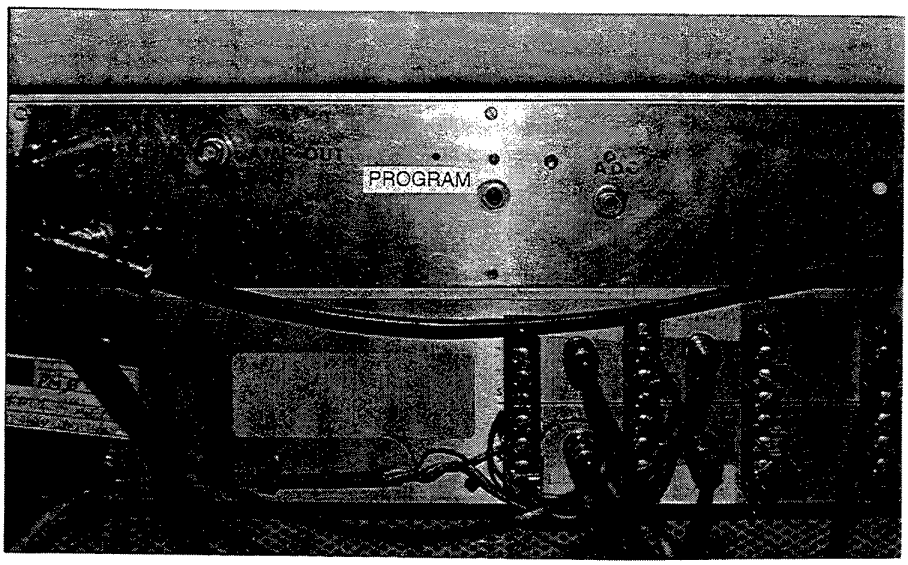


Figure A4. View of front panel.

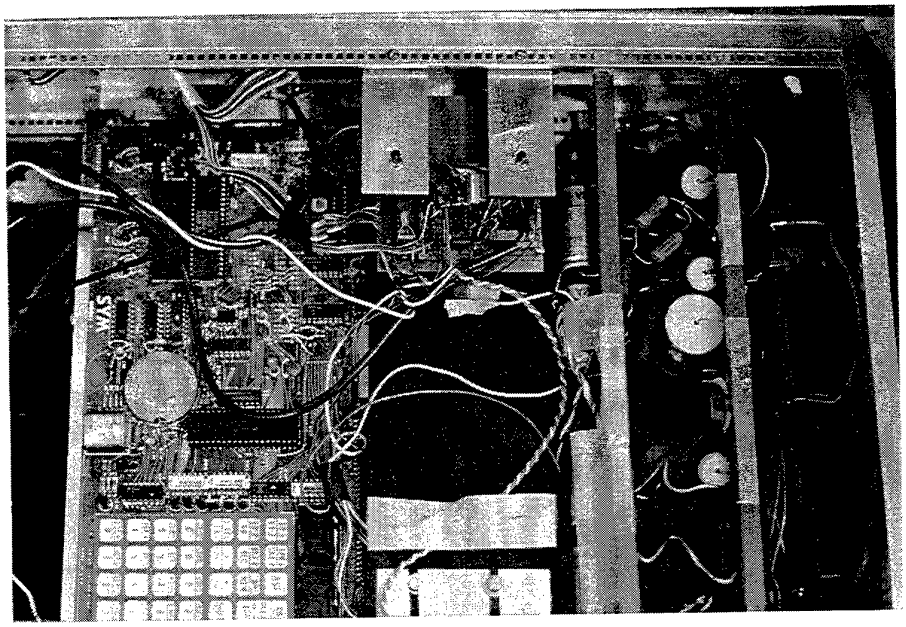
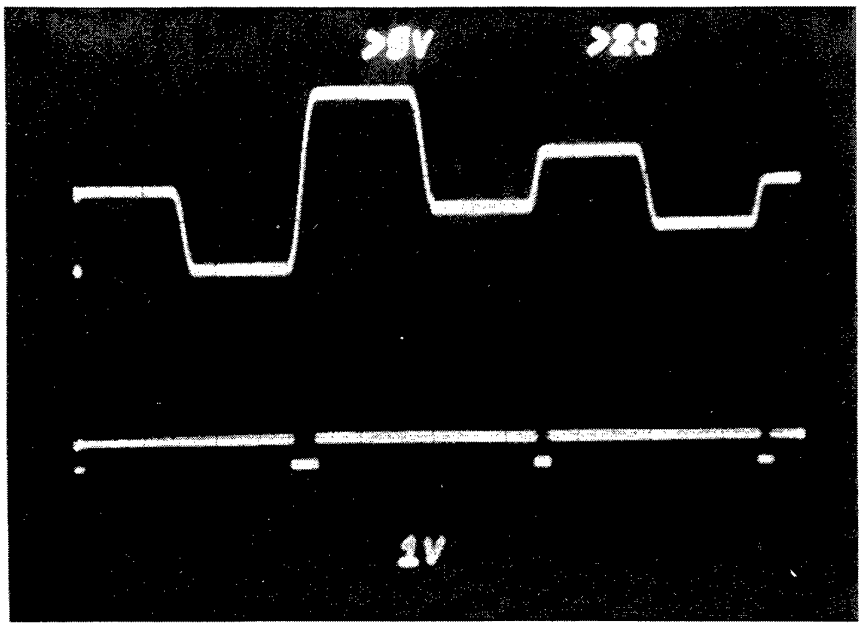


Figure A5. Layout of microprocessor and ancillary boards.



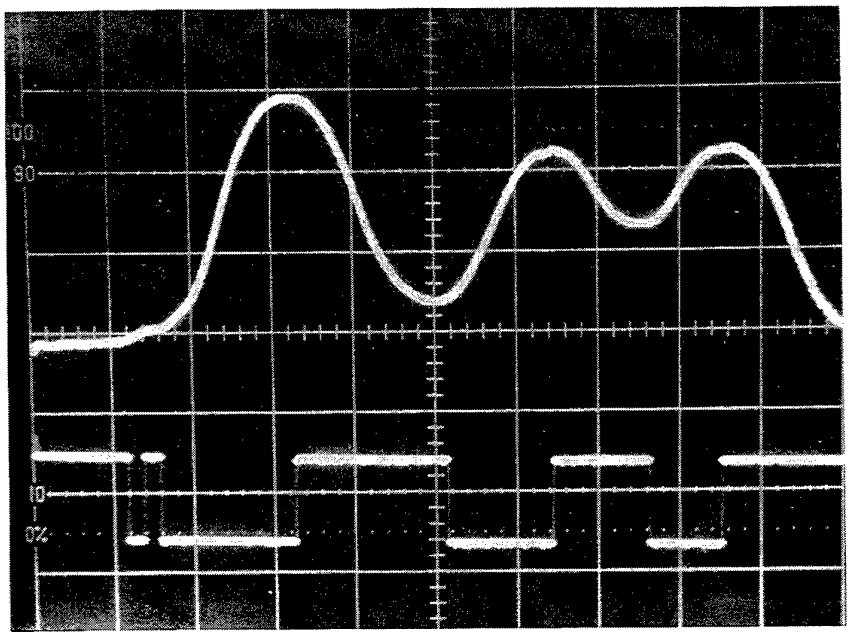


Figure A6. Oscilloscope traces.
(A) Arbitrary machine waveform (top trace) and corresponding analyser output (lower trace).
(B) F/A-18 spectrum load sequence (top trace) and corresponding analyser output (lower trace).

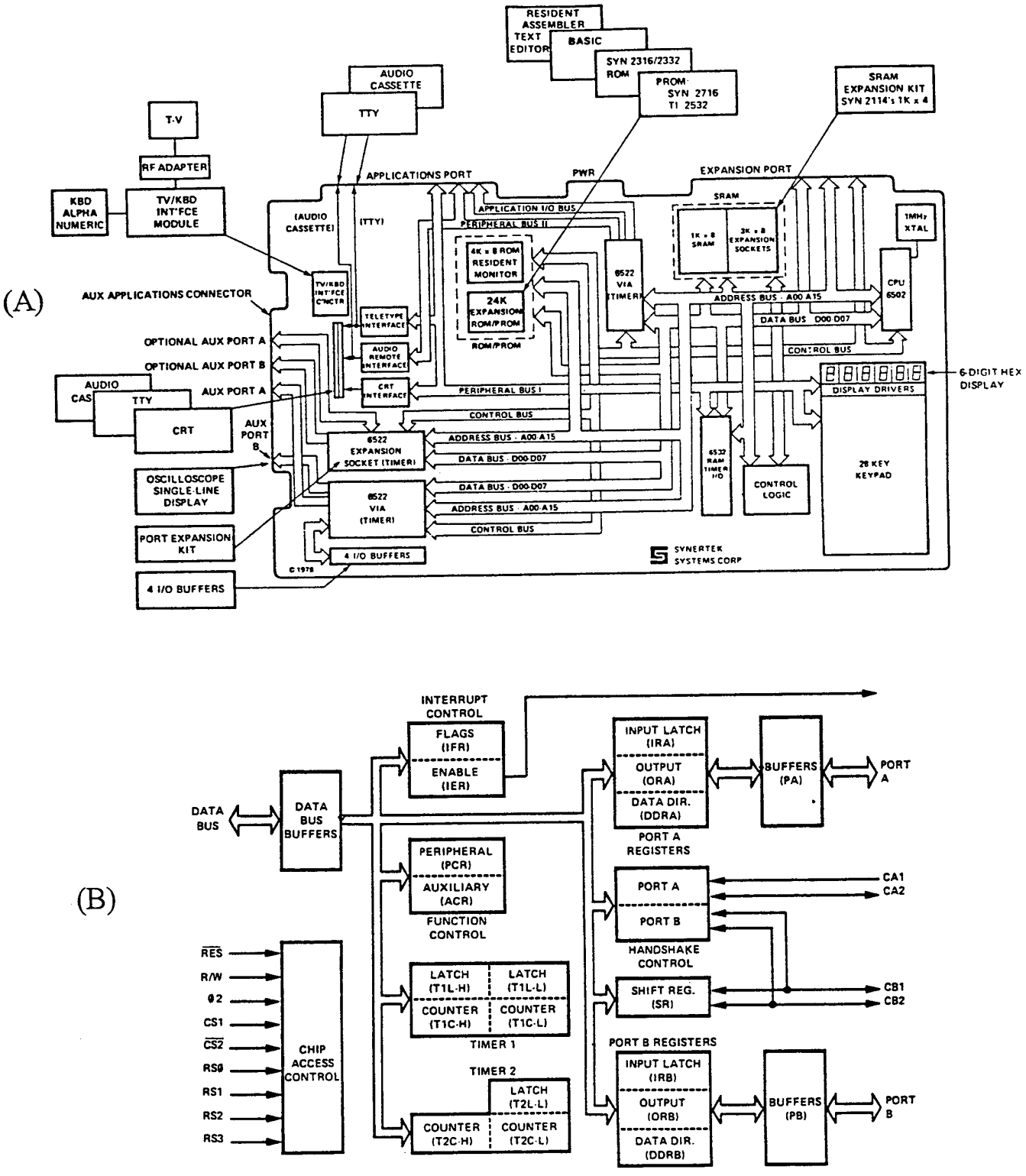
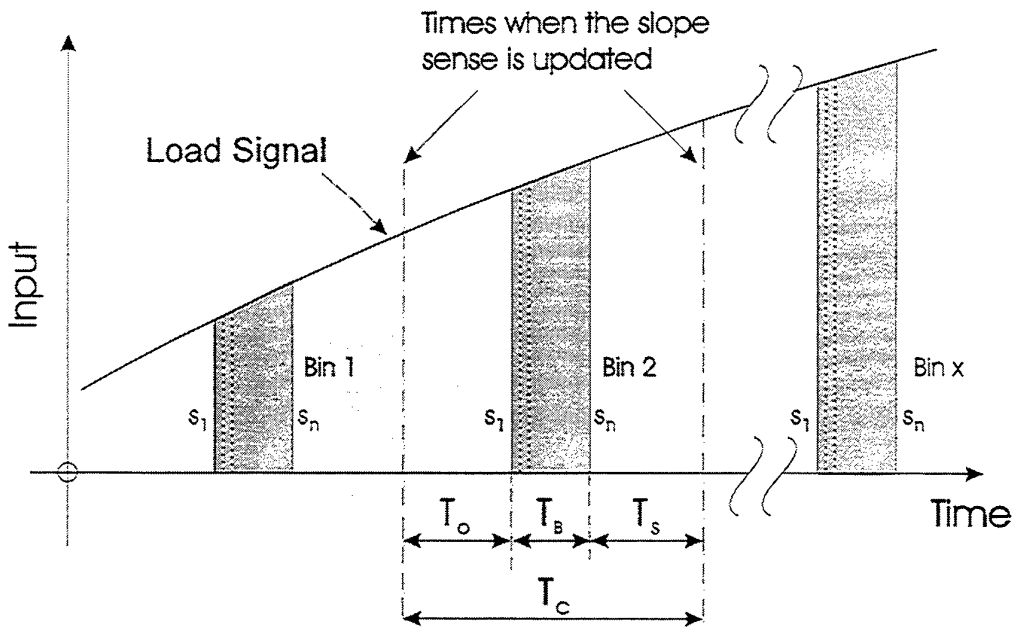


Figure A7. Functional block diagrams
(A) SYM processor board
(B) 6522 Versatile Interface Adapter



s_1 first sample in bin

s_{LAST} last sample in bin

Figure A8. Timing

Appendix B

GRAD Program Code and Flow Diagram

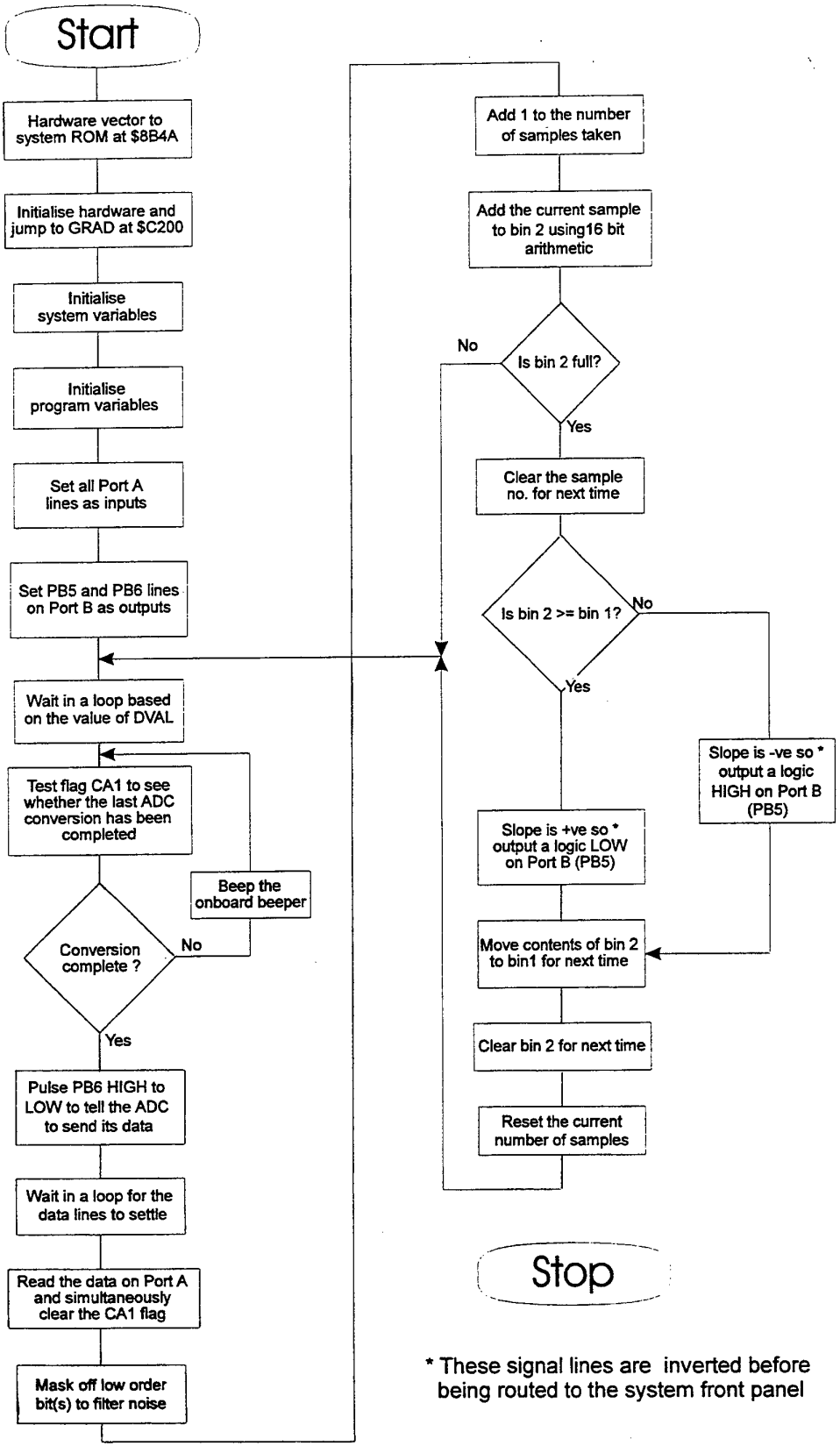


Figure B1. Flow chart for program GRAD.

Program Grad

This program determines the sign (+ve or -ve) of an analog signal in real time and signals the result as logic high for a -ve slope and vice versa for +ve slope. This signal is brought out to a connector after being transistor buffered and inverted so that the final outcome is +ve for a +ve slope and vice versa.

The analog signal is continuously converted into 8 bit data samples by a free running analog-to-digital converter (f~500kHz) and read via an 8 bit 6522 peripheral interface adaptor. Samples are accumulated with 16 bit precision and stored as the current bin until a set sample number limit is reached after which time the accumulated value is compared with the previous value in the previous bin.

This program is written in 6502 machine code for a Synertek Systems SYM-1 microprocessor board running at a clock speed of 1 MHz and uses some ROM resident routines. The software resides on an 2754D EPROM which is vectored to boot automatically when power is applied to the system.

Legend

$ Preceding a number means that number is hexadecimal.

Immediate addressing mode. The data byte is the byte following the instruction.

% Binary representation.

System ROM Calls

Address	Subroutine Name	Description
$8188	SAVER	Saves all 6502 registers on the stack. At return the stack looks like: F Top of stack A X Y
$81C4	RESALL	Jumped to after SAVER. Restores all registers from stack and performs a RTS.
$8972	BEEP	Beeps the onboard beeper.

Variables

Hexadecimal Address	Mnemonic	Description
$0000	ALOW	Low order byte of bin 1.
$0001	AHIGH	High order byte of bin 1.
$0002	BLOW	Low order byte of bin 2. Bin 2 holds the most up to date samples.
$0003	BHIGH	High order byte of bin 2. Bin 2 holds the most up to date samples.
$0004	SAMPNO	The most recent no. of samples to be found in bin 2.
$0005	LIMIT	The no. of samples needed to make up a "full" bin.
$0006	DVAL	The default value used for a timing loop.

Input/Output Ports

Port A

Address	Bits							
$A801	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
	MSB							LSB

Description

This is the address of an 8 bit I/O register which is used to read data samples after A/D conversion. All bits are set as inputs.

Port B

Address	Bits							
$A800	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
	MSB							LSB

This is the address of another 8 bit I/O register which has two uses. PB5 is used as the signal line which indicates whether the current slope is +ve or -ve. This bit is logic 0 for a +ve slope and 1 for a -ve slope. The signal is passed to a connector labelled SIG. OUT after being inverted to give the correct sign sense to the user.

PB6 is another output line and it is used to trigger the ADC to begin sending data to Port A. Once triggered the ADC continues to send data in free running mode.

PB0, PB1, PB2, PB3, PB4, and PB7 are not used.

CA1 Flag

The CA1 flag is a hardware control line at address $A80C. This line controls an interrupt flag in the interrupt flags register at address $A80D. The interrupt flag at $A80D is set by an active transition (LOW to HIGH) on the CA1 line and cleared by either a read or write of Port A. CA1 is physically connected to the INTR line on the A/D converter (pin 5) so that a transition will occur on this line whenever the A/D converter has valid data. ie. the last A/D conversion is complete. For further information on interrupt control see the data sheet supplied, Appendix ??

Interrupt Flags Register

Address	Bits							
$A80D	IFR7	IFR6	IFR5	IFR4	IFR3	IFR2	IFR1	IFR0
	X	X	X	X	X	X	Set by an active transition on the CA1 pin. Cleared by a read or write of Port A.	X

Peripheral Control Register

	Bits							
$A80C	PCR7	PCR6	PCR5	PCR4	PCR3	PCR2	PCR1	PCR0
	X	X	X	X	X	X	CA1 signal line. Connects to INTR on the ADC0801 converter, pin 5.	X

Program Code

Address Label	Hex Address	Hex Machine Code	Mnemonic	Description
BEGIN	$C200	A2 FF	LDA #$FF	
		9A	TXS	
		A9 CC	LDA #$CC	Disable power-on-reset
		8D 0C A0	STA $A00C	
		A9 04	LDA #$04	
		48	PHA	
		28	PLP	
		20 AF C2	JSR ACCESS	Open up access to system RAM. Necessary !
	$C20F	A9 00	LDA #$00	
		8D 03 A8	STA $A803	Set all port A bits as inputs
		85 00	STA $0000	Initialise some program variables
		85 02	STA $0002	
		85 01	STA $0001	
		85 03	STA $0003	
		85 04	STA $0004	
		8D 0E A8	STA $A80E	Clear all interrupt enable bits. ie disable all interrupts except NMI's.
	$C221	A9 60	LDA #$60	Set the default samples per full bin to 96 (decimal).
		85 05	STA $0005	
		A9 15	LDA #$15	
		85 06	STA $0006	
		A9 60	LDA #%0110 0000	Set bits high in the data direction register ($A802) to make PB5 and PB6 output lines. All other lines are set as inputs.
		8D 02 A8	STA #$A802	

START	$C22D	A4 06	LDY #$06	Set the wait interval.
		20 A4 C2	JSR DELAY	Now wait a while.
TEST		A9 02	LDA #$02	
		2C 0D A8	BIT $A80D	Test the CA1 flag bit. CA1 (IFR1) is set high when an A/D conversion has been completed.
		D0 06	BNE READY	Branch to READY only when a conversion has been completed.
		20 72 89	JSR BEEP	Beep the onboard beeper to indicate a possible problem.
		38	SEC	
		B0 F3		Jump back to TEST for more.
READY	$C240	A9 02	LDA #$02	Reset the CA1 flag for next time.
		8D 0D A8	STA $A80D	
		A9 40	LDA #%0100 0000	Now force a transition on PB6 to tell the A/D converter to put its data on Port A ($A801).
		0D 00 A8	ORA $A800	First send the bit HIGH.
		8D 00 A8	STA $A800	
		49 40	EOR #%0100 0000	Then LOW.
		8D 00 A8	STA $A800	
	$C252	AD 01 A8	LDA $A801	Now read the data that's arrived.
		29 FC	AND #%1111 1100	Mask off unneeded bits.
		E6 04	INC $0004	Increment the sample count.
		18	CLC	And add the current data to the bin 2. Low byte first followed by High byte.
		65 02	ADC $0002	
		85 02	STA $0002	
		A5 03	LDA $0003	
		69 00	ADC $0000	
	$C261	85 03	STA $0003	
		A6 04	LDX $0004	Now test to see whether bin 2 is full.

		E4 05	CPX $0005	
		F0 02	BEQ OK	Branch to OK if bin 2 is full.
		D0 C2	BNE START	Otherwise go back for more.
OK		A9 00	LDA #$00	Now reset the sample count.
		85 04	STA $0004	
		A5 03	LDA $0003	Now compare bin 2 with bin 1.
	$C272	C5 01	CMP $0001	High bytes first.
		F0 0C	BEQ EQ1	Branch to EQ1 if High bytes are equal.
		90 12	BCC HIGH	Branch to HIGH if bin 1 is > bin 2. ie. slope is -ve.
LOW		A9 DF	LDA #%1101 1111	Slope is +ve. Put a LOW on PA5. Remember - this signal is inverted later so that final result is HIGH is for +ve and LOW is for -ve.
		2D 00 A8	AND $A800	
		8D 00 A8	STA $A800	
		B0 10	BCS MOVE	Carry flag is always set here so this is the same as a jump to MOVE.
EQ1	$C282	A5 02	LDA $0002	High bytes are equal. Now compare the low bytes.
		C5 00	CMP $0000	
		F0 F0	BEQ LOW	If bytes are equal branch to LOW. ie zero slope is taken as +ve.
		B0 EE	BCS LOW	If the carry flag is set then bin 2 is > bin 1 so branch to LOW.
		A9 20	LDA #%0010 0000	Put a HIGH on PA5. After inversion this will indicate a -ve slope.
		0D 00 A8	ORA $A800	
		8D 00 A8	STA $A800	
MOVE	$C292	A5 03	LDA $0003	Housekeeping. We're finished with the current data. Now move bin 2 to bin 1 for the next time through.
		85 01	STA $0001	
		A5 02	LDA $0002	

```
                    85 00           STA  $0000
ZERO                A9 00           LDA  #$00       Now clear bin 2 for next time.
                    85 02           STA  $0002
                    85 03           STA  $0003
                    F0 8C           BEQ  START      This is a jump to START.
          $C2A2     EA              NOP
                    EA              NOP
```

****

This subroutine keeps the CPU busy for an amount of time. On entry register Y must contain a value for the required delay. Each call to this routine consumes 51Y+5clock cycles.

****

```
DLY       $C2A4     A2 09           LDX  #$09       A deliberate time wasting subroutine
LP1                 CA              DEX
                    D0 FD           BNE  LP1
                    88              DEY
                    D0 F8           BNE  DLY
                    60              RTS
```

```
*****************************************************************************************
```

This is a copy of a ROM resident subroutine called ACCESS which provides access to the SYM-1's 'system' RAM between addresses $A600-$A67F. Access to system RAM is required by various ROM routines and if this call is not made unpredictable results could occur.

```
*****************************************************************************************
```

	$C2AD	EA	NOP	
		EA	NOP	
ACCESS	$C2AF	20 88 81	JSR SAVER	Call the system ROM routine which saves all internal registers.
		AD 01 AC	LDA $AC01	Open up access to the system RAM.
		09 01	ORA #$01	
		8D 01 AC	STA $AC01	
		AD 03 AC	LDA $AC03	
		09 01	ORA #$01	
		8D 03 AC	STA $AC03	
	$C2C2	4C C4 81	JMP RESALL	Reverses what SAVER does. Retores all registers from the stack and performs an RTS

```
*****************************************************************************************
```

		EA	NOP	
		EA	NOP	

```
*****************************************************************************************
```

This subroutine beeps the onboard beeper, scans the onboard keypad for key presses, and also refreshes (lights up) the onboard LED display so key presses are made visible.

```
*****************************************************************************************
```

		20 88 81	JSR SAVER	Save all registers.
		A9 0D	LDA #$0D	
		20 F2 C2	JSR CONFIG	Set up I/O for onboard beeper.
		A2 40	LDX #$40	X register sets the number of times to loop around.
BE1	$C2D1	A9 08	LDA #%0000 1000	Turn on the onboard LED display.
		8D 02 A4	STA $A402	

```
                    20 EA C2        JSR  BE2          Wait a while.
                    A9 06           LDA  #$0000 0110  Turn off the LED display
                    8D 02 A4        STA  $A402
                    20 EA C2        JSR  BE2          Wait a while.
          $C2E1     CA              DEX
                    D0 ED           BNE  BE1          Loop back if not done.
                    20 F0 C2        JSR  CON          Scan the keypad.
                    4C C4 81        JMP  RESALL       Restore all registers.
*************************************************************************************
This routine wastes some CPU cycles. ie it provides a timed delay.
*************************************************************************************
BE2       $C2EA     A0 28           LDY  #$28         Waste some CPU cycles
AGAIN               88              DEY
                    D0 FD           BNE  AGAIN
                    60              RTS
*************************************************************************************

CON       $C2F0     A9 01           LDA  #$01         Configure for keypad input.
*************************************************************************************
This is a copy of a ROM subroutine of the same name. Must be called prior to attempting certain I/O operations.
On entry the value in the accumulator register determines which I/O device is being set up. eg when:

A= $01, sets up input to be from the onboard hex keypad

A = $0D, sets up the onboard beeper for output
*************************************************************************************
CONFIG              20 88 81        JSR  SAVER
                    A0 01           LDY  #$01
                    AA              TAX
RPT                 BD C8 8B        LDA  $8BC8, X
          $C301     99 02 A4        STA  $A402, Y
                    BD C6 8B        LDA  $A400, Y
```

```
99 00 A4        STA  $A400, Y
CA              DEX
88              DEY
10 F0           BPL  RPT
4C C4 81        JMP  RESALL
```

****

Appendix C

Diagnostics

Included here are some suggestions for troubleshooting common problems.

1. If, after powering up the unit, and pressing the PROGRAM button, a continuous beeping sound is heard it means that the ADC has not started. The technical specification for the ADC0801 does not guarantee that the ADC will 'free run' at power-on. The momentary action button labelled ADC is, therefore, provided on the system unit front panel to start the converter.
2. If the beeping persists after pressing this button, then the ADC is either not functioning or a fault on the analog circuit board is preventing the ADC's "conversion completed" signal from reaching the CPU via the I/O port.
3. If the beeper is silent but the system does not output gradient information then there is most likely a fault related to the microcomputer itself.

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A Microprocessor-Based Gradient Analyser for F/A-18 Bulkhead Spectrum Loading

Leopold Sponder

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19. ABSTRACT This report describes a specially designed instrument that was used during a full scale fatigue test of an F/A-18 bulkhead to support the acquisition and analysis of acoustic emission (AE) data for the investigation of crack initiation and growth. This device, developed by the author, comprises both hardware and software and generates binary data in real time that indicates the sign of the gradient of an applied spectrum load signal. This design overcomes the inherent limitations of conventional analog slope detection methods applied to slowly varying aperiodic waveforms.				